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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/730,817	12/08/2003	Daniel Owen	1801270.00134US1	4224

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EXAMINER	
KANG, INSUN	

ART UNIT	PAPER NUMBER
2193	

NOTIFICATION DATE	DELIVERY MODE
03/06/2008	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/730,817	OWEN ET AL.	
	Examiner	Art Unit	
	INSUN KANG	2193	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 February 2008*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,4,6-18,20,23,25-38,41,43-58 and 80-85* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 4, 6-18, 20, 23, 25-38, 41, 43-58, 80-85* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the RCE amendment filed 2/1/2008.

2. As per applicant's request, claims 1, 4, 6-8, 10-13, 15-18, 20, 23, 25-27, 29-32, 34-38, 41, 44, 45, 47-50, 52-55, 58, 82, and 83 have been amended. Claims 1, 4, 6-18, 20, 23, 25-38, 41, 43-58, 80-85 are pending in the application. The indicated allowability of claims 10-13, 15-18, 29-32, 34-37, 47-50, 52-58, 80-82, 84 and 85 is withdrawn in view of the newly discovered reference(s) to Srivastava and Fujii. Rejections based on the newly cited reference(s) follow.

Claim Rejections - 35 USC § 101

3. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claims 38, 41, and 43-58 are non-statutory because it is directed to a translator apparatus that does not have any physical structural elements. The recited processor and memory are not tied to the apparatus but to the target computing environment. With no other structure in the independent claim to rely on, the alleged "apparatus" of the claims comprising program instructions such as decoding mechanism (compiler), type determining mechanism (instructions) etc turns out to be an abstract idea for being a computer program per se, and, thus, does not fit within the definition of the categories of patentable subject matter set forth in § 101. Therefore, the claims are non-statutory. Recommendation: A translator apparatus having a processor.

The following link on the World Wide Web is for the United States Patent And Trademark Office (USPTO) policy on 35 U.S.C. §101. The following link on the World

Wide Web is for the United States Patent And Trademark Office (USPTO) policy on 35 U.S.C. §101.

<http://www.uspto.gov/web/offices/pac/dapp/opla/preognotice/guidelines101_20051026.pdf>

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

5. Claims 9-18, 28-37, 46-58, 80-82, 84, and 85 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 9, 14, 28, 33, 46, and 51, recite the limitation "the plurality of possible types" in the claims. There is insufficient antecedent basis for this limitation in the claims. Interpretation: the type of nodes.

Per claims 16 (line 9), 35 (line 10), 53 (line 9), it is unclear to which "target architecture specialized conversion function" it is referring. Interpretation: "the target architecture specialized conversion function."

Claims 57, 81, and 85 recite the limitation "the polymorphic node" in the claims. There is insufficient antecedent basis for this limitation in the claim. Interpretation: the polymorphic nodes.

As per claims 10-13, 15, 17, 18, 29-32, 34, 36, 37, 47-50, 52, 54-56, 58 80, 82, and 84 these claims are rejected for dependency on the above rejected parent claims.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

7. Claims 1, 4, 7, 8, 14, 20, 23, 26, 27, 33, 38, 41, 44, 45, and 51 are rejected under 35 U.S.C. 102(b) as being anticipated by Srivastava et al. (US 6,609,248) hereafter Srivastava.

Per claim 1:

Srivastava discloses:

- decoding a plurality of instructions in the program code (i.e. "After the instructions in the code blocks have been translated,," col. 7 lines 20-21)
- determining which type of nodes to generate in an intermediate representation for each of the decoded instructions in the program code (i.e. "Once the code and data blocks are identified, an IR creation process 212 evaluates each platform-dependent instruction on a block-by-block basis," col. 6 lines 65-67),
- including determining that one or more of the decoded instructions require base nodes having basic RISC-like functionality which provides an expanded representation of semantics of the decoded instructions (i.e. "For RISC

…architectures,…instructions can be easily translated into a single platform-neutral IR instruction," col. 7 lines 3-6),

- and one or more of the decoded instructions require complex nodes having complex CISC-like functionality which provides a compact representation of semantics of the decoded instructions (i.e. "On the other hand, CICS…contain complex instructions that provide the function of multiple instructions," col. 7 lines 5-8);
- generating the intermediate representation of the decoded instructions using the determined types of nodes, including generating the base nodes and the complex nodes in the intermediate representation from the respective decoded instructions (i.e. "the platform-dependent instructions that have a single platform-neutral IR instruction counterpart are translated into that platform-neutral instruction, while complex instructions are replicated as-is within the IR through an extended version of the basic IR instruction," col. 7 lines 9-20);
- generating the target code from the intermediate representation and executing the target code on the target computing system (i.e. "Blocks of instructions that were originally written for one architecture can be translated from the intermediate representation into platform-specific instructions for a different architecture," col. 14 lines 52-55; the EXE' 203 in Fig. 2A is a target specific executable for a target system, col. 8 lines 22-30).

Per claim 4:

Srivastava further discloses:

- wherein the base nodes are generic across a plurality of possible subject computing architectures (i.e. "a single platform-neutral IR instruction," col. 7 lines 1-3).

Per claim 7:

Srivastava further discloses:

- wherein each of the complex nodes may be decomposed into a plurality of the base nodes to represent the same semantics of an instruction in the decoded program code (i.e. "*CISC* (Complex Instruction Set Computer) …contain complex instructions (col. 7 lines 5-10) which are composed with basic blocks that can be discomposed back into basic blocks).

Per claim 8:

Srivastava further discloses:

- generating the complex nodes only for those features which are correspondingly configurable on the subject computing architecture (i.e. "A replicated complex instruction is marked with a signature that denotes its architecture," col. 7 lines 13-16).

Per claim 14:

Srivastava further discloses:

- wherein the plurality of possible types of nodes further include architecture specific nodes (i.e. "set of platform-specific instructions to perform the same

function as the original, complex instruction," col.8 lines 63-65).

Per claims 20, 23, 26, 27, and 33, they are the medium versions of claims 1, 4, 7, 8, and 14, respectively, and are rejected for the same reasons set forth in connection with the rejection of claims 1, 4, 7, 8, and 14 above.

Per claims 38, 41, 44, 45, and 51, they are the apparatus versions of claims 1, 4, 7, 8, and 14, respectively, and are rejected for the same reasons set forth in connection with the rejection of claims 1, 4, 7, 8, and 14 above.

Claim Rejections - 35 USC § 103

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

9. Claims 6, 25, and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srivastava et al. (US 6,609,248) hereafter Srivastava.

Per claim 6:

Srivastava does not explicitly teach that the determining step includes that the program code includes immediate type instructions in which a constant operand value is encoded into the instruction itself in an immediate field and in response determining that the immediate type instructions require the complex nodes. However, a CISC-like functionality includes such immediate type instructions. Therefore, it would have been obvious for one having ordinary skill in the art to modify Srivastava's disclosed system to

include specific CISC functionalities such as immediate type instructions in the determining step so that such CISC-like instructions can be "replicated as-is within the IR through an extended version of the basic IR instruction (col. 7 lines 5-20)."

Per claim 25, it is the medium version of claim 6, respectively, and is rejected for the same reasons set forth in connection with the rejection of claim 6 above.

Per claim 43, it is the apparatus version of claim 6, respectively, and is rejected for the same reasons set forth in connection with the rejection of claim 6 above.

10. Claims 9, 28, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srivastava et al. (US 6,609,248) hereafter Srivastava in view of Lattner et al. ("The LLVM Instruction Set and Compilation Strategy," 8/9/2002).

Per claim 9:

Srivastava does not explicitly teach that the plurality of possible types of IR nodes further include polymorphic nodes. However, Lattner teaches such nodes was known in the pertinent art, at the time applicant's invention was made, to perform a single operation on several different types of operands (i.e. "LLVM instructions are polymorphic," a single instruction…can operate on several different types of operands," page 4, section 3.2, third paragraph)." It would have been obvious for one having ordinary skill in the art to modify Srivastava's disclosed system to incorporate the teachings of Lattner. The modification would be obvious because one having ordinary skill in the art would be motivated to reduce "the number of distinct opcodes (page 4, section 3.2, third

paragraph)" by replicating such polymorphic nodes "as-is within the IR (col. 7 lines 5-20)."

Per claim 28, it is the medium version of claim 9, respectively, and is rejected for the same reasons set forth in connection with the rejection of claim 9 above.

Per claim 46, it is the apparatus version of claim 9, respectively, and is rejected for the same reasons set forth in connection with the rejection of claim 9 above.

11. Claims 10-13, 29-32, 47-50, 56-58, 80-82, 84, and 85 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srivastava et al. (US 6,609,248) hereafter Srivastava, in view of Lattner et al. ("The LLVM Instruction Set and Compilation Strategy," 8/9/2002), and further in view of Fujii et al. (US Pg. Pub. 2004/0015888) hereafter Fujii.

Per claim 10:

Srivastava and Lattner do not explicitly teach that the program code is dynamically translated into the target code for execution on the target computer system. However, Fujii teaches such a dynamic binary translation was known in the pertinent art, at the time applicant's invention was made, to dynamically translate a program at runtime ("dynamic binary translation,"0010). It would have been obvious for one having ordinary skill in the art to modify Srivastava and Lattner's disclosed system to incorporate the teachings of Fujii. The modification would be obvious because one having ordinary skill in the art would be motivated to perform the binary translation from the intermediate representation disclosed in Srivastava and Lattner only when the code is actually discovered at runtime.

Lattner further discloses:

-generating the intermediate representation to include the polymorphic nodes,

wherein the polymorphic nodes each contain a function pointer to a function of the target computing system specific to a particular instruction in the program code (i.e. page 8, 3.8 Function calls and exceptions; "all call instructions take a function pointer to invoke").

Per claim 11:

Lattner further discloses: generating the polymorphic nodes when the features of the target computing system would cause the semantics of a particular instruction in the program code to be lost if realized as the base (i.e. "LLVM instructions are polymorphic," a single instruction…can operate on several different types of operands," page 4, section 3.2, third paragraph)."

Per claim 12:

Lattner further discloses: each polymorphic node is specific to a combination of a particular instruction in the program code and a function of the target computing system (i.e. page 2, The LLVM approach, first paragraph).

Per claim 13:

Srivastava in view of Lattner further discloses: said determining step further comprises identifying an instruction in the program code which corresponds an instruction on a list of polymorphic instructions to be realized as the polymorphic nodes; and said generating step generates the polymorphic nodes only for those instructions in the program code corresponding to those on the list of polymorphic instructions (i.e. col.

6 lines 65-67; "Procedures are determined by…using information provided in the PDB file," col. 7 lines 20-37).

Per claim 80:

Lattner further discloses: said generated polymorphic nodes specify the registers to be allocated during target code generation (i.e. page 3, 3.1. Overview of the LLVM architecture, lines 1-6).

Per claim 81:

Lattner further discloses: wherein said generated polymorphic nodes are utilized in generic kernel optimizations by inferring information from the function pointer in the polymorphic node which may otherwise be indeterminable from the polymorphic node (i.e. page 1, last paragraph; page 14, see 5.5 LLVM optimizing linker, third paragraph).

Per claim 82:

Lattner further discloses: wherein when a subject instruction corresponds to an instruction on the list of polymorphic instructions, said intermediate representation generating step generates either the polymorphic nodes or the base nodes for those subject instructions corresponding to those on the list of polymorphic instructions (i.e. page 4, 3.2. Three address code, second paragraph; 3.3. Static Single Assignment form, first paragraph).

Per claims 29-32, 84, and 85, they are the medium versions of claims 10-13, 80-82, respectively, and are rejected for the same reasons set forth in connection with the rejection of claims 10-13, 80-82 above.

Per claims 47-50 and 56-58, they are the apparatus versions of claims 10-13, 80-82, respectively, and are rejected for the same reasons set forth in connection with the rejection of claims 10-13, 80-82 above.

12. Claims 15-18, 34-37, 52-55, and 83 are rejected under 35 U.S.C. 103(a) as being unpatentable over Srivastava et al. (US 6,609,248) hereafter Srivastava, in view of Fujii et al. (US Pg. Pub. 2004/0015888) hereafter Fujii.

Per claim 15:

Srivastava does not explicitly teach that the program is dynamically translated into the target code for execution on the target computing system having a target architecture. However, Fujii teaches such a dynamic binary translation was known in the pertinent art, at the time applicant's invention was made, to dynamically translate a program at runtime ("dynamic binary translation,"0010). It would have been obvious for one having ordinary skill in the art to modify Srivastava's disclosed system to incorporate the teachings of Fujii. The modification would be obvious because one having ordinary skill in the art would be motivated to perform the binary translation from the intermediate representation disclosed in Srivastava only when the code is actually discovered at runtime.

Srivastava further discloses: generating the intermediate representation to include the architecture specific nodes which are specific to a particular combination of the subject computing architecture and the target architecture (i.e. col. 8 lines 55-65).

Per claim 16:

Srivastava further discloses: initially representing all of the instructions in the program code as subject architecture specific nodes, where each subject architecture specific node corresponds to a respective instruction in the program code (i.e. col. 6 lines 55-65); determining whether an instruction in the program code is one in which to provide a target architecture specialized conversion function; (i.e. col. 6 lines 65-67);

converting the subject architecture specific nodes into target architecture specific nodes for those instructions determined to provide a target architecture specialized conversion function (i.e. col. 8 lines 56-65);

generating the base nodes from the remaining subject architecture specific nodes which are not identified as providing a-the target architecture specialized code generation function (i.e. col.7 lines 1-5).

Per claim 17:

Srivastava further discloses: generating the target code from the target architecture specific nodes, wherein the target code is specialized for the target architecture (i.e. col. 8 lines 55-65).

Per claim 18:

Srivastava further discloses: generating the target code from the base nodes, wherein the target code is not specialized for the target architecture (i.e. col. 7 lines 1-5).

Per claims 34-37, they are the medium versions of claims 15-18, respectively, and are rejected for the same reasons set forth in connection with the rejection of claims 15-18 above.

Per claims 52-55, they are the apparatus versions of claims 15-18, respectively, and are rejected for the same reasons set forth in connection with the rejection of claims 15-18 above.

Per claim 83:

Srivastava does not explicitly teach that the translation is a dynamic binary translation from the subject program code as binary machine code of a subject instruction set architecture into the target code as binary machine code of a target instruction set architecture. However, Fujii teaches such a dynamic binary translation was known in the pertinent art, at the time applicant's invention was made, to dynamically translate a program at runtime ("dynamic binary translation,"0010). It would have been obvious for one having ordinary skill in the art to modify Srivastava's disclosed system to incorporate the teachings of Fujii. The modification would be obvious because one having ordinary skill in the art would be motivated to perform the binary translation from the intermediate representation disclosed in Srivastava only when the code is actually discovered at runtime.

Response to Arguments

13. Applicant's arguments with respect to claims 1, 20, and 38 have been considered but are moot in view of the new ground(s) of rejection.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to INSUN KANG whose telephone number is (571)272-3724. The examiner can normally be reached on M-F 8:30-5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lewis A. Bullock, Jr. can be reached on 571-272-3759. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Insun Kang/
Examiner, Art Unit 2193